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Sensing Voltage Transients Using Built-in Voltage Sensor

Prepared for: Design Review 2, VLSI Design - ECE6332

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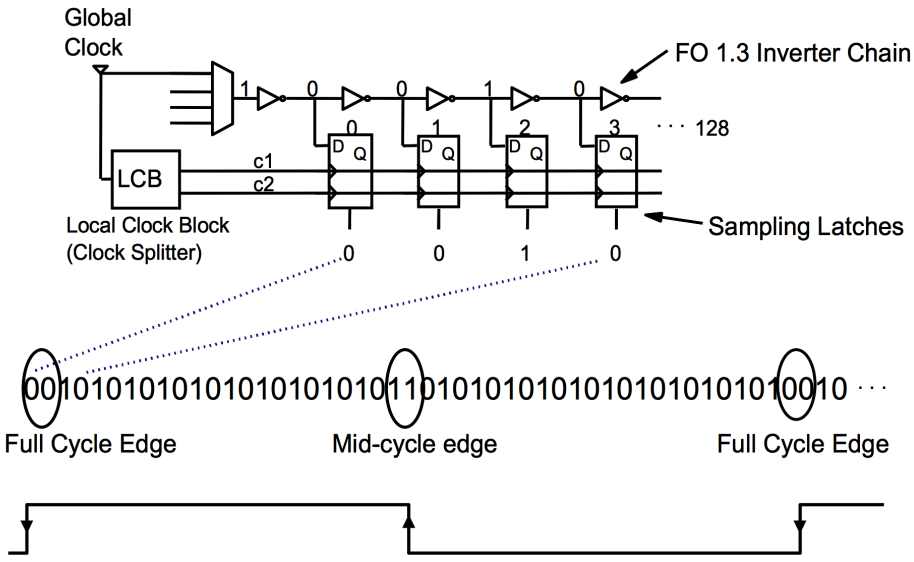
University of Virginia

Design Review 2

More on Related Work

One of the key components in our voltage sensor is the delay line, which is a voltage sensitive element. In this project, potential applications of the voltage sensor will be investigated if time permits at the end of the semester. In [1], IBM proposed using similar delay line to measure clock jitter and clock skew. Unlike the delay elements used in our design, the SKITTER sensor proposed in [1] uses a single inverter as the basic delay element. The design also uses latches to sample the voltage on the delay line. Instead of getting a sequence of '1' or '0', the SKITTER gets a sequence of "10". If there happens to be large jitter or clock skew, abnormal bits like "11" or "00" will appear in the digital code. The circuit that captures the edge is shown in the following figure. A clock splitter splits the global clock into two so that at each rising and falling edge of the clock the latch can sample one time at each of the events. Besides measuring the jitter and SKITTER sensor also takes into account the effect of voltage changes on the clock jitter and skew, because the delay line is very sensitive to voltage changes and it also reflect voltage changes.



Simulation Results

Up to now, we have simulated the three basic delay elements (buffer, open latch and transmission gate), the delay line, the TDC and the voltage sensor. Detailed simulation results are shown as follows.

Buffer

The simulation of the buffer has already been done in the last design review. Here only the schematic and simulation results are shown for the comparison made later.

Table 1. Voltage-delay profile of a buffer (using the FreePDK 45nm technology library).

voltage (V)	rising time (ps)	falling time (ps)	tp (ps)
0.7	40.7	40.8	40.75
0.8	35.5	34.8	35.15
0.9	32.8	35.3	34.05
1	29.6	29.9	29.75
1.1	29.3	28.6	28.95
1.2	29	28.3	28.65
1.3	27.2	27.6	27.4
1.4	26.7	27.6	27.15
1.5	25	26	25.5

Transmission Gate

Transmission gate is another basic delay element that could be used in the delay line. A simulation of the transmission gate's voltage-delay relationship has been performed in the last design review, but something was wrong with that simulation. Here the simulation of a transmission gate is repeated and the new simulation results are shown. The simulation circuits are shown in Figure 1, and the simulation results are shown in Table 2. From the simulation results, we see that like buffer a transmission gate also has similar voltage-delay relationship. Generally, when voltage goes higher, the delay of the transmission gate is smaller.

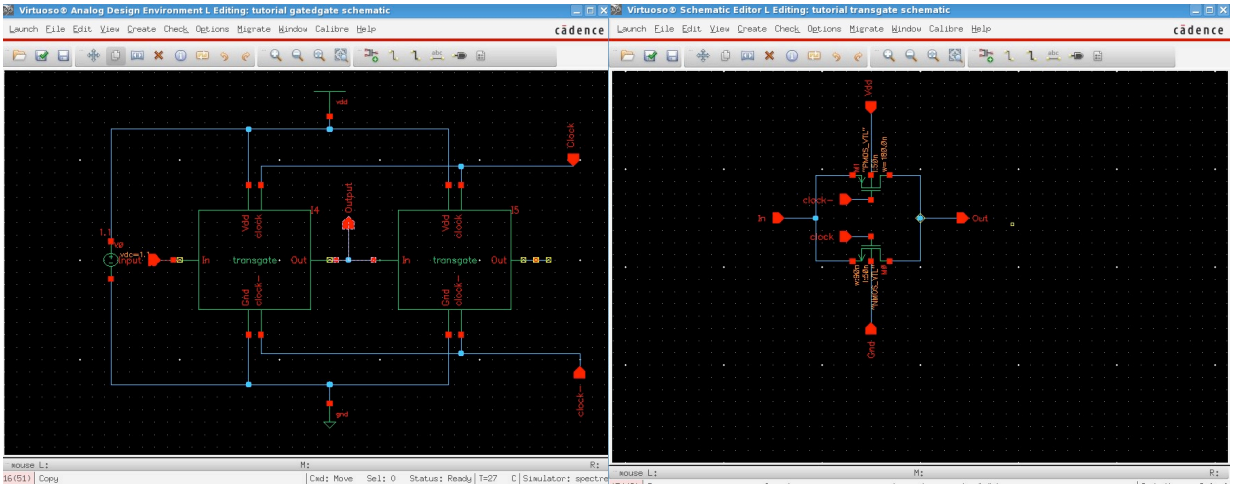


Figure 1. Simulation circuits of a transmission gate.

voltage (V)	rising time (ps)	falling time (ps)	tp (ps)
0.7	31.6	33.2	32.4
0.8	25.8	30.3	28.05
0.9	27.4	34.7	31.05
1	25.4	31	28.2
1.1	26.4	29.7	28.05
1.2	23.7	30.4	27.05
1.3	23.7	28.7	26.2
1.4	23.1	27.1	25.1
1.5	22.1	26.7	24.4

Table 2. Simulation results of a transmission gate.

Open Latch

The simulation results of an open latch has already been shown in the last design review. Here only the simulation results are shown for the comparison made later.

Table 3. Voltage-delay relationship of an open latch

voltage (V)	rising time (ps)	falling time (ps)	tp (ps)
1.5	60.6	62.36	61.48
1.4	59	66	62.5
1.3	64.6	61.9	63.25
1.2	67.3	68.31	67.805
1.1	70	68.78	69.39
1	69.7	70.35	70.025
0.9	80.4	77.87	79.135
0.8	78.5	80.05	79.275
0.7	100.1	99.79	99.945

Comparison of Delay Elements

The plot of the voltage-delay relationships of the three basic delay elements are shown in Figure 2, 3, 4. From the figures,

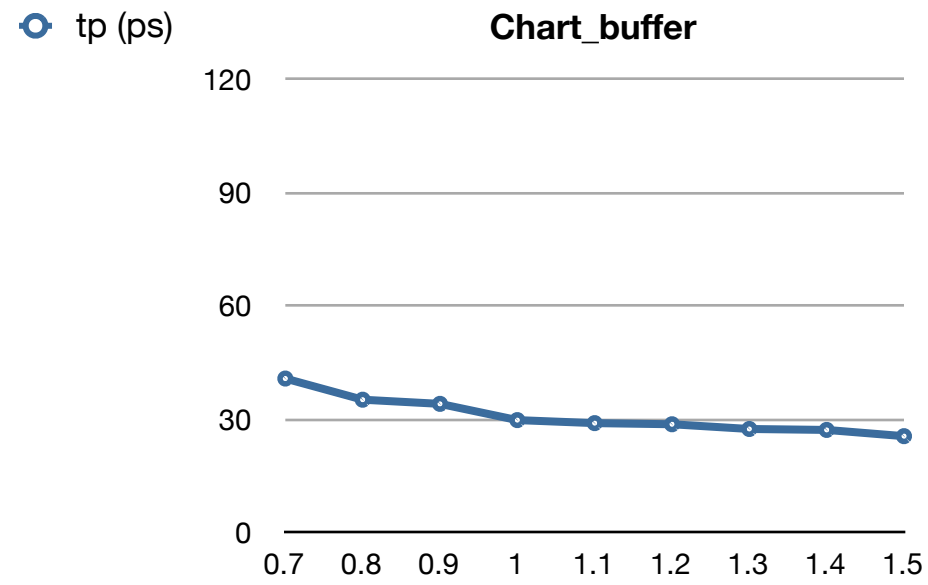


Figure 2. Voltage-delay relationship of the buffer.

it can been seen that all the three basic delay elements have similar voltage-delay relationship, that is the delay decreases as the voltage increases. However, they also have significant difference. The delay of the open latch is about twice the delay of the buffer or the transmission gate under the same voltage. In addition, the open latch is more sensitive to voltage changes, as can be seen in the figures that the slope of the voltage-delay curve of the open latch is steeper than

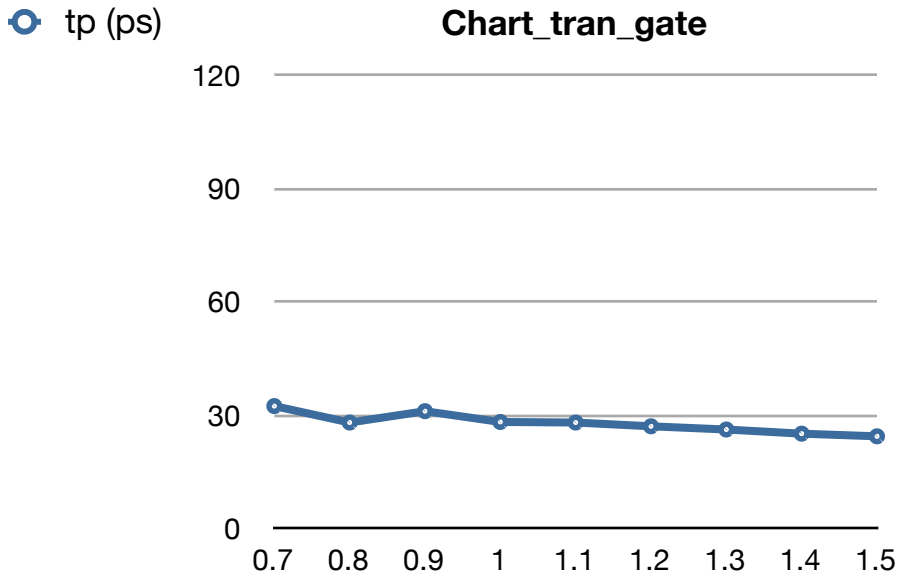


Figure 3. Voltage-delay relationship of the transmission gate.

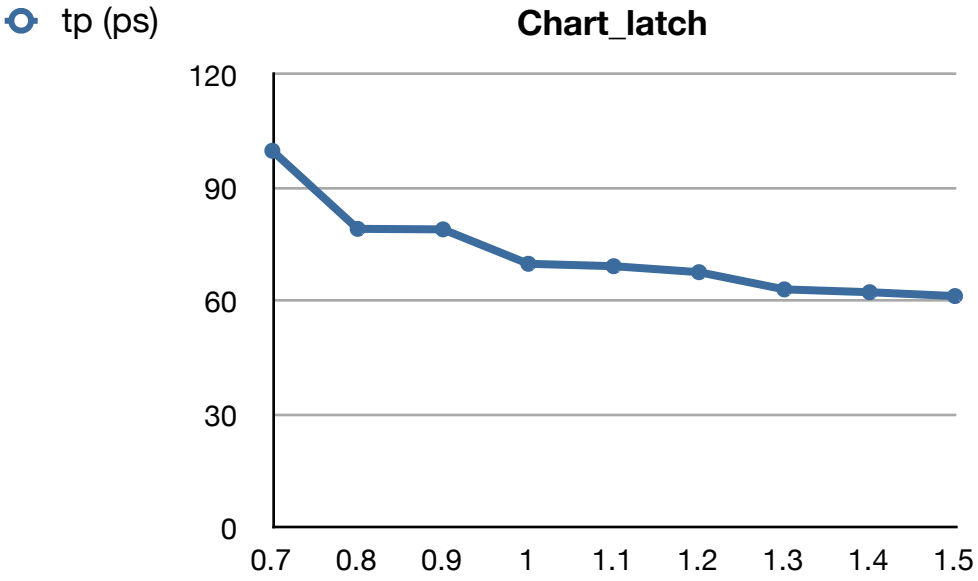


Figure 4. Voltage-delay relationship of the open latch.

that of the buffer or the transmission gate. This is very useful in that we can use the open latch as the delay line that senses the voltage changes, and use the buffer as the delay elements in the TDC. This is because that the delay line is the key component that senses the voltage changes and it is required to be as more sensitive as possible, and the delay

element in the TDC is used to convert delay to voltage and it is required to be as less sensitive to voltage as possible. Another thing to notice is that as the voltage becomes very low, the delay elements are more sensitive to voltage changes, which can be seen from the fact that the slope of the curves are steeper at the lower voltage end. Since the voltage-delay relationship is not strictly linear, we need to correct that when calibrating the voltage sensor.

For the later sensor design, we are going to use the buffer as the delay element in the TDC and use the open latch as the delay element in the delay line.

Design Goals

Before we proceed to the actual design of the sensor, we would like to first set the design goals of the sensor. We want the sensor be able to sense voltage as low as 0.7 volts and as high as 1.5 volts, that is a range of 0.8 volts. We set the resolution of the sensor to be 1bin/10mV. Here 'bin' is used to indicate a single digit in the final digital codes. 1bin/10mV means that when voltage drops by 10mV, the edge of the output digital binary code will shift by one digit. Hence to achieve a range of 0.8mV, a total number of 80 bins are needed, which means 80 delay elements and 80 flip-flops. These are too much hardware resource consumption for a single sensor. As a compromise, we use 64 bins in the sensor design and this means smaller measuring range, but it has already covered most of the common and extreme cases. Thus the actual measuring range of the sensor is 640mV and the TDC consumes 64 buffers and flip-flops.

Next we need to calculate the length of the delay line. The sensitivity of the buffer and the open latch is calculated and shown in Table 4. At nominal voltage, we want the input signal of the delay line in the TDC propagates to the middle of the line, allowing equal ranges for both overshoot and undershoot. Based on the sensitivity information and the delay information above, we calculated the number of open latches needed in the sensing delay line, which is around 100. For a fine tuning of the input of the sensing delay line, we can use phased shifted clock signal.

Table 4. Sensitivity of the buffer and open latch.

	No. Transis-tors	delay/voltage
buffer	4	1.333ps/100mV
latch	8	2.542ps/100mV

Table 5. Design goals of the voltage sensor.

Design Goals								
minimum (V)	**nominal (V)**	**maximum (V)**	**range (V)**	**resolution**	**No. of bins**	**actual range**	**No. of buffers**	**No. of latches**
0.7	1.1	1.5	0.8	1 bin/10mV	64	640mV	64	100

Delay Line

The delay line consists of a number of open latches as the basic delay elements. The schematic of the delay line is shown in Figure 5 and Figure 6. Figure 6 shows a delay line of only 10 delay elements, and a delay line of 100 delay elements consists of 10 delay line with 10 delay elements. This is to save the workload of drawing the delay line schematic. We performed a simulation on the delay line and the simulation circuit is shown in Figure 7.

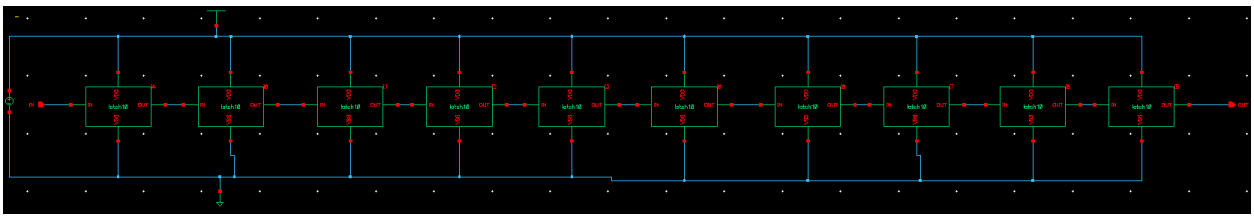


Figure 5. A delay line with 10 delay elements.

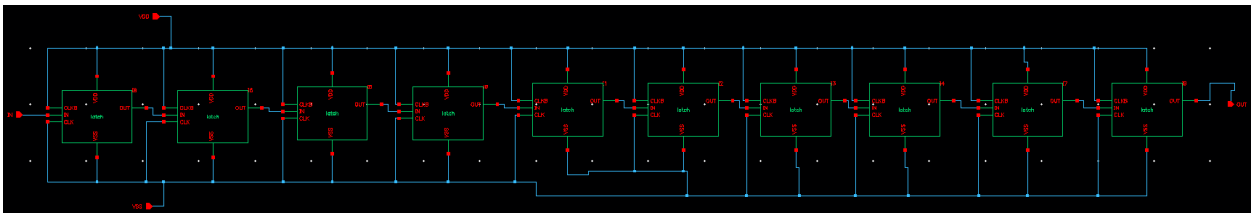


Figure 6. A delay line with 10 delay lines with 10 delay elements.

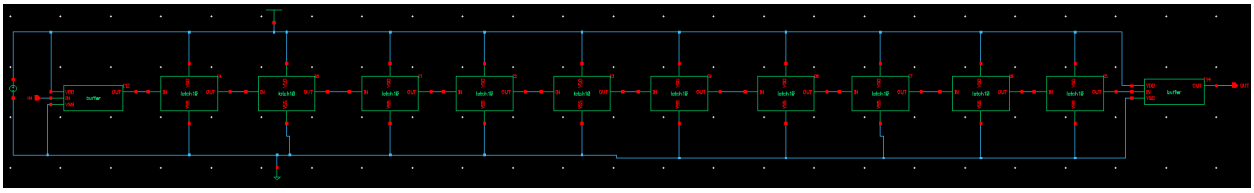


Figure 7. Test circuit schematic of the delay line.

The simulation results of the delay line with 100 delay elements is shown in Table 6. The average voltage-delay relationship is calculated and shown in the table. The simulation waveform is shown in Figure 8.

Table 6. Simulation results of the delay line with 100 delay elements.

delay line with 100 open latches				
voltage (V)	**rising time (ns)**	**falling time (ns)**	**tp (ns)**	**delay/voltage (ns/100mV)**
0.7	4.717	4.707	4.712	0.29775
1.1	2.828	2.855	2.8415	
1.5	2.334	2.326	2.33	

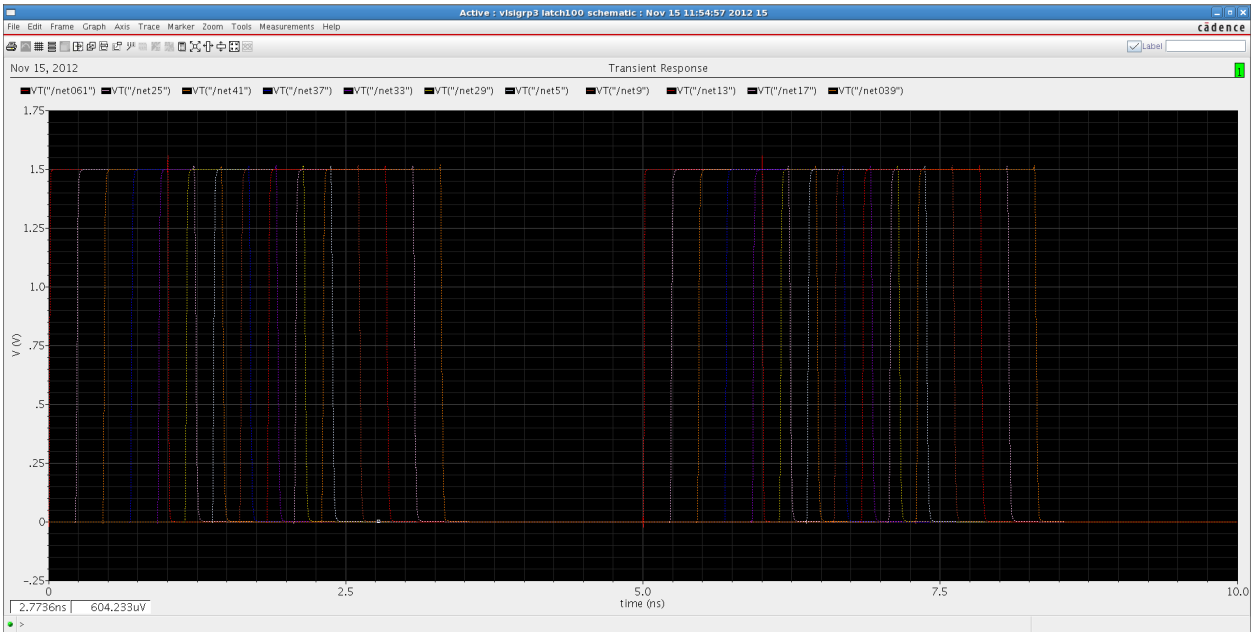


Figure 8. Simulation waveform of the delay line.

Time to Digital Converter

The delay element used in the TDC is the buffer, which is not that sensitive to voltage changes compared with the open latch. Flip-flops are used to sample the delay elements. A schematic of the TDC with 8 bins is shown in Figure 9, and a schematic of the TDC with 64 bins is shown in Figure 10. The TDC with 64 bins consists of 8 small TDCs with 8 bins. This is to reduce the workload of drawing the circuit schematic.

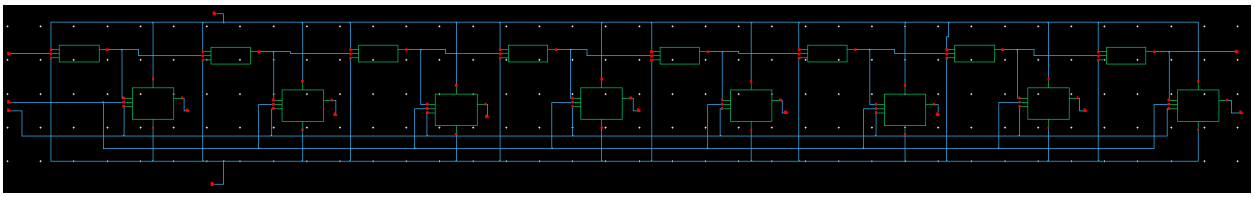


Figure 9. Schematic of a TDC with 8 bins.

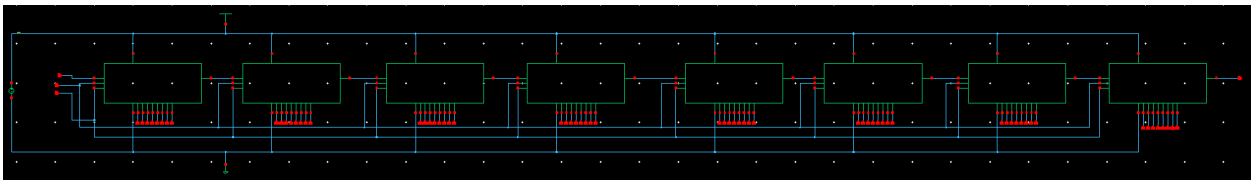


Figure 10. The schematic of a 64-bin TDC, consisting of 8 8-bin TDCs.

A static simulation of the 64-bin TDC was also performed. In the simulation, the clock cycle is 2ns. The input to the TDC is also a periodic signal but is phased shifted in order to create a delay between the input and the clock. This time difference is then converted to a digital code by the TDC. The simulation results are shown in Figure 11 and Figure 12. The simulation verified that the function of the TDC is correct. The TDC is simulated at different voltage levels, and simulation shows the edge shift of the output digital code. The simulation shows that the TDC is more sensitive to voltage when the voltage level is at the lower end, while it is less sensitive when the voltage level is at the higher end. In lower voltages, the number of shifted bins is 1bin/29mV on average, and in higher voltages, the number of shifted bins is 1bin/67mV on average. This result is shown in Table 7. Our design goal is to achieve a resolution of 1bin/10mV. Obviously relying on the TDC alone could not achieve this goal, because the buffers in the TDC is not sensitive enough to voltage changes. Thus an extra delay line that is more sensitive to voltage changes is required.

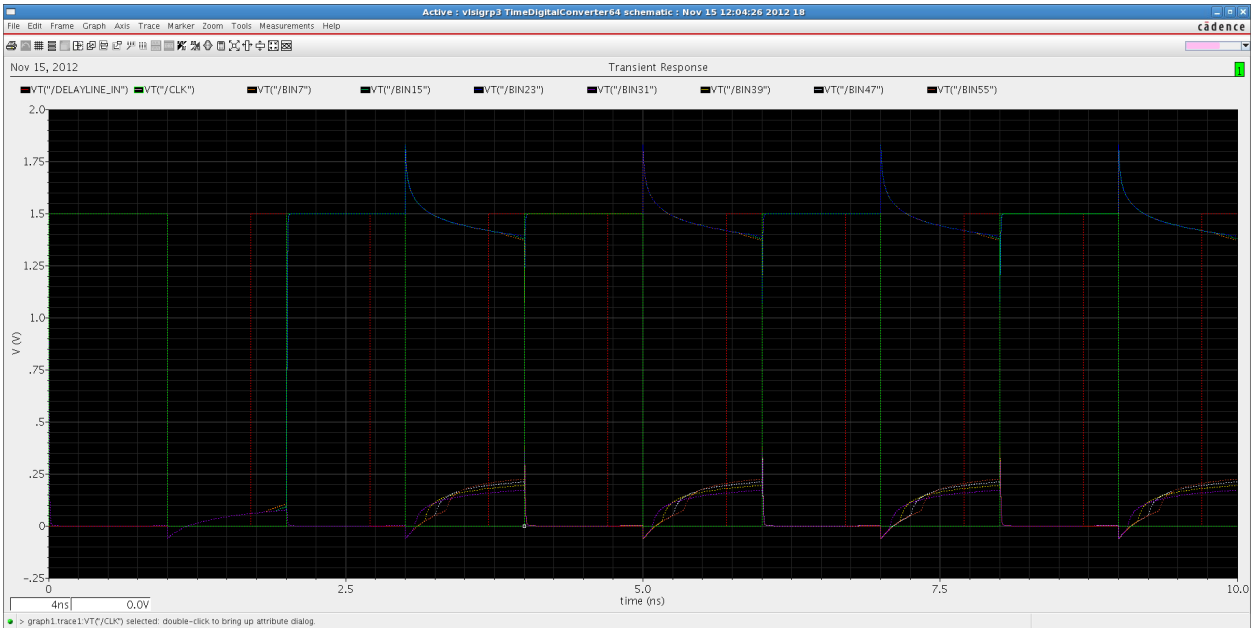


Figure 11. Simulation results of the TDC. It shows clock, input, delayed signal, and digital codes.

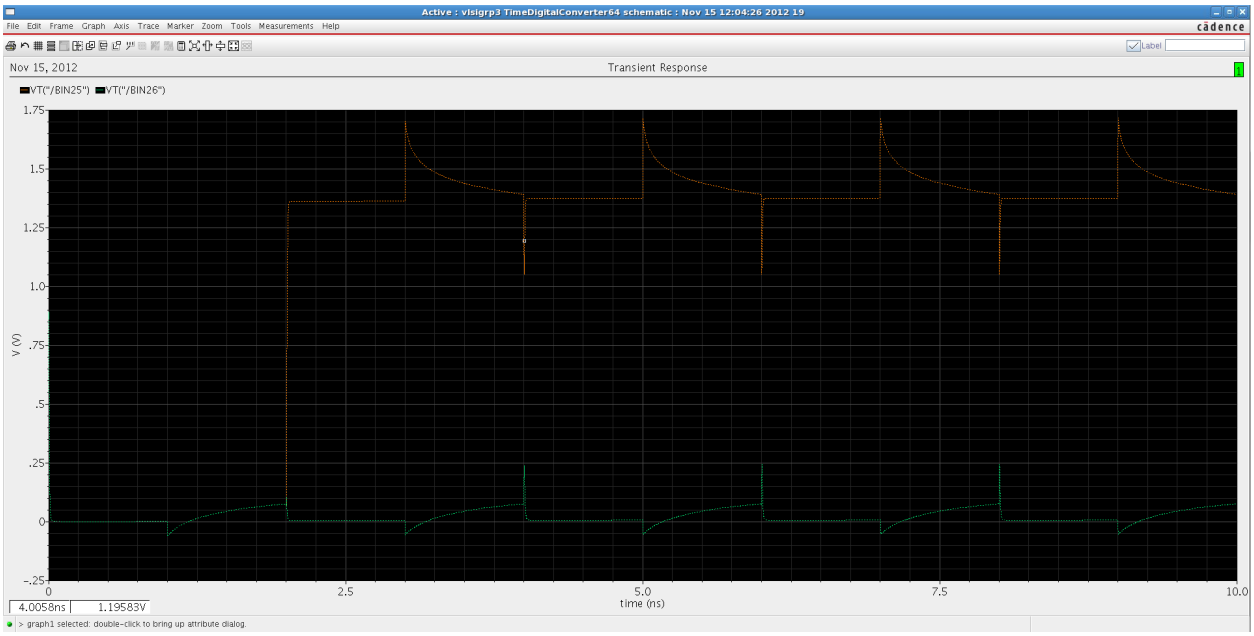


Figure 12. Simulation results of TDC. It shows the edge of the digital code, which is between bin 25 and bin 26.

Table 7. Delay of TDC measured as the number of bins shifted.

Delay of TDC			
voltage (V)	**transition bin**	**No. of shift bins**	**bin/voltage**
0.7	23,24	14	1bin/29mV
1.1	37,38	0	
1.5	43,44	6	1bin/67mV

Voltage Sensor

The voltage sensor consists of two key components: an extra delay line and a TDC. Its schematic is shown in Figure 15. A preliminary static simulation is performed on the sensor. We did not build the system that models the power network for the time being and we will do this later in the project to emulate a real power supply environment. At present, we focus on the static behavior of the voltage sensor and try to fine tuning it. The final sensor design may deviate from the one specified in the design goal.

In the simulation, the sensor is first fine tuned under nominal voltage so that the edge of the digital code is centered to allow maximum measuring range. The input signal to the delay line is phased shifted compared with the clock signal to adjust the edge of the digital code. Then higher and lower voltages are applied to simulate the sensor. Under nominal voltage (1.1V), the edge of the binary digital code is at bin 37 and bin 38. When voltage increased to 1.2V, the edge shifted to between bin 53 and bin 54. When voltage further increased to 1.3V, the sensor is already saturated and overflew. This means that the sensing delay line is too long the sensor is too sensitive to voltage changes. The resolution of the sensor under this design is 1bin/6.25mV on average, which is higher than our design goals. This sensor design has a narrow range and we need to decrease the sensitivity of the sensing delay line. Figure 16 and Figure 17 show the simulation results of the voltage sensor under nominal voltage.

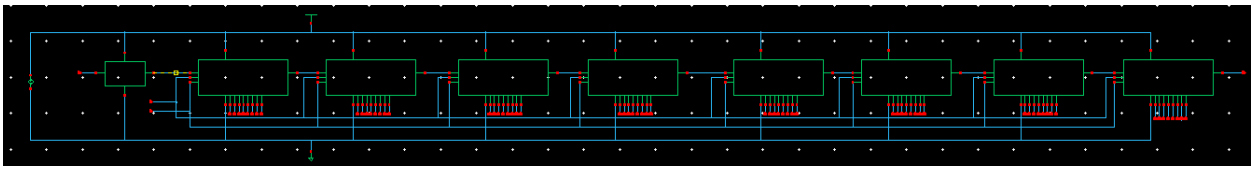


Figure 13. Schematic of the voltage sensor.

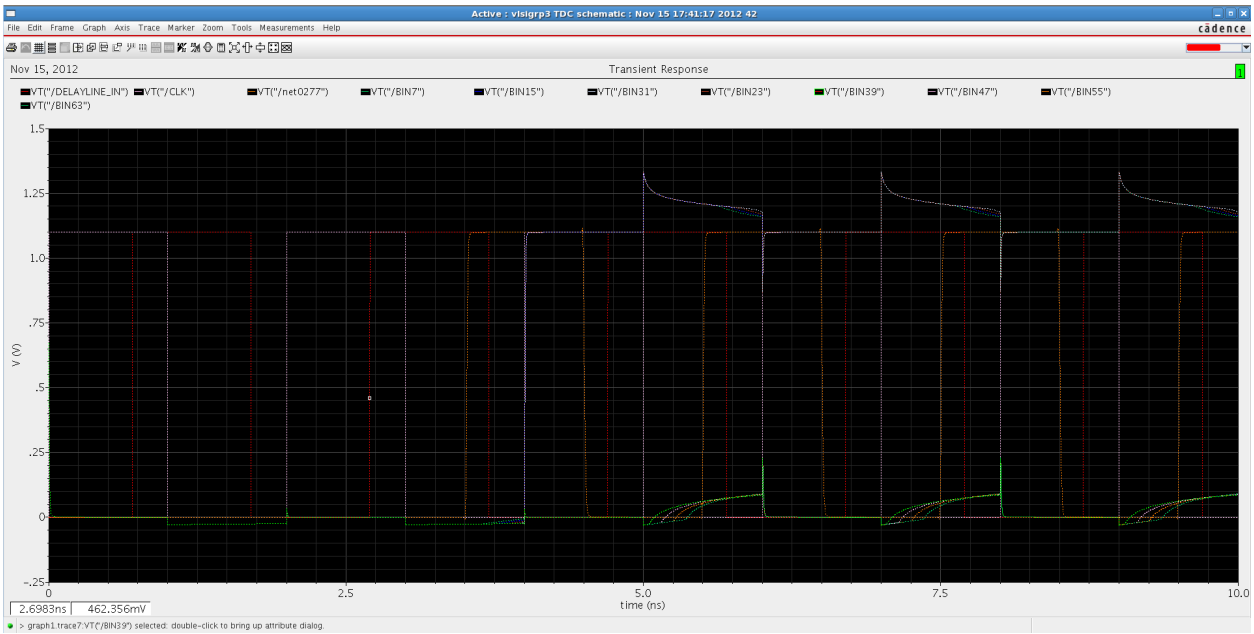


Figure 14. Simulation results of the voltage sensor under nominal voltage (1.1V).

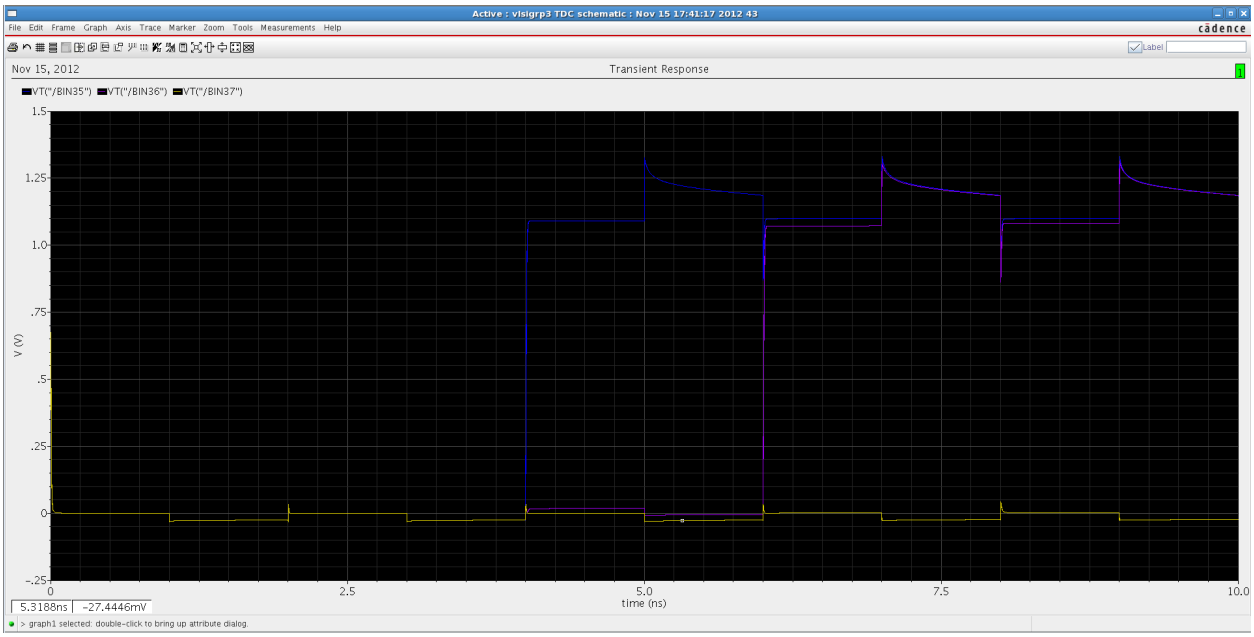


Figure 15. Edge of the binary digital code of the sensor in simulation.

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Progress and Remaining Tasks

So far, we have simulated the three basic delay elements and get their voltage-delay relationships. We have completed design of the sensor including the delay line and the TDC. In addition, we performed some preliminary simulations on the voltage sensor. Right now the sensor is too sensitive to voltage changes and we still need to fine tune the sensor to let meet our design goals as closer as possible.

In the remaining part of the project, we will adjust the sensitivity of the sensor and its range. Besides the static simulation having done so far, we will model the power supply network and perform dynamic simulations. This power supply may be emulated by a network of inductance and capacitances and current sources. When the design of the sensor is finalized, we will layout the sensor and get more accurate simulations.

Project Timeline

The project is scheduled to be finished within the course time span. A timeline of the project is shown in Table 2. So far, we have progressed to week 11, model voltage transient and evaluate the voltage sensor. In the following weeks, we will finish the evaluation and layout the voltage sensor.

Table 8. Timeline of the project.

Tasks	Weeks							
	8	9	10	11	12	13	14	15
Simulate delay elements (buffer, transmission gate, open latch, RC)	✓							
Complete TDC designs and simulate it		✓						
Complete the voltage sensor design and simulate it			✓					
Model voltage transient and evaluate the voltage sensor				✓				
Layout the voltage sensor					✓			
Perform post-layout simulation of the voltage sensor						✓		
Write paper							✓	
Write final report and prepare for presentation								✓

Task Breakdown

The work was done by Zhe Song and Wei Zhang. Zhe did the simulation of the buffer and the transmission gate and analyzed their voltage-delay relationships. Wei simulated the open latch and analyzed its voltage-delay relationship. Wei built the delay line and simulated the delay line. Zhe built the TDC and draw the schematic. Wei simulated the TDC and

made corresponding evaluation. Wei also built the voltage sensor and draw the schematic. Preliminary simulations on the voltage sensor was also done by Wei. And Wei wrote the report.

Conclusion

We investigated the voltage-delay relationship of the three basic delay elements and finished most of the design of the sensor by far. We also have done corresponding simulations on the delay elements, the TDC and the voltage sensor. Our final objective is to design a voltage sensor that meets our expectations and can effectively sense the voltage transients.

References

[1] R. Franch, P. Restle, N. James, W. Huott, J. Friedrich, R. Dixon, S. Weitzel, K. Van Goor, G. Salem, “On-chip timing uncertainty measurements on IBM microprocessors,” International Test Conference, 2007.